

Analog Frequency Multiplier (XO)

**Technical Document
(Preliminary)**

PRODUCT DESCRIPTION

PhaseLink's Analog Frequency Multipliers™ AFMs are the industry's first 'Balanced Oscillator' utilizing analog multiplication of the fundamental frequency (at double or quadruple frequency), combined with an attenuation of the fundamental of the reference crystal, without the use of a phase locked loop, in CMOS technology.

PhaseLink's patent pending PL66X family of AFM products can achieve up to 320 MHz output with practically no jitter or phase noise deterioration.

The PL66X AFM products are specifically designed for low-cost high performance applications. Designed to accept a low frequency input, these devices allow the usage of a low-cost fundamental or 3rd overtone crystal to reduce the overall system cost, while PhaseLink's non phase locked loop AFM function allows x2 or x4 multiplication of the input frequency for high performance outputs, ranging from 60 MHz -320 MHz. This feature permits significant crystal cost reduction while offering higher performance unattainable with other technologies, at comparable cost.

PL66X-XX family of products utilize a low-power CMOS technology and are housed in a 16-pin TSSOP, and 16-pin 3x3 QFN. Additionally, the AFM products are capable of producing a differential PECL, LVDS, or single-ended CMOS output.

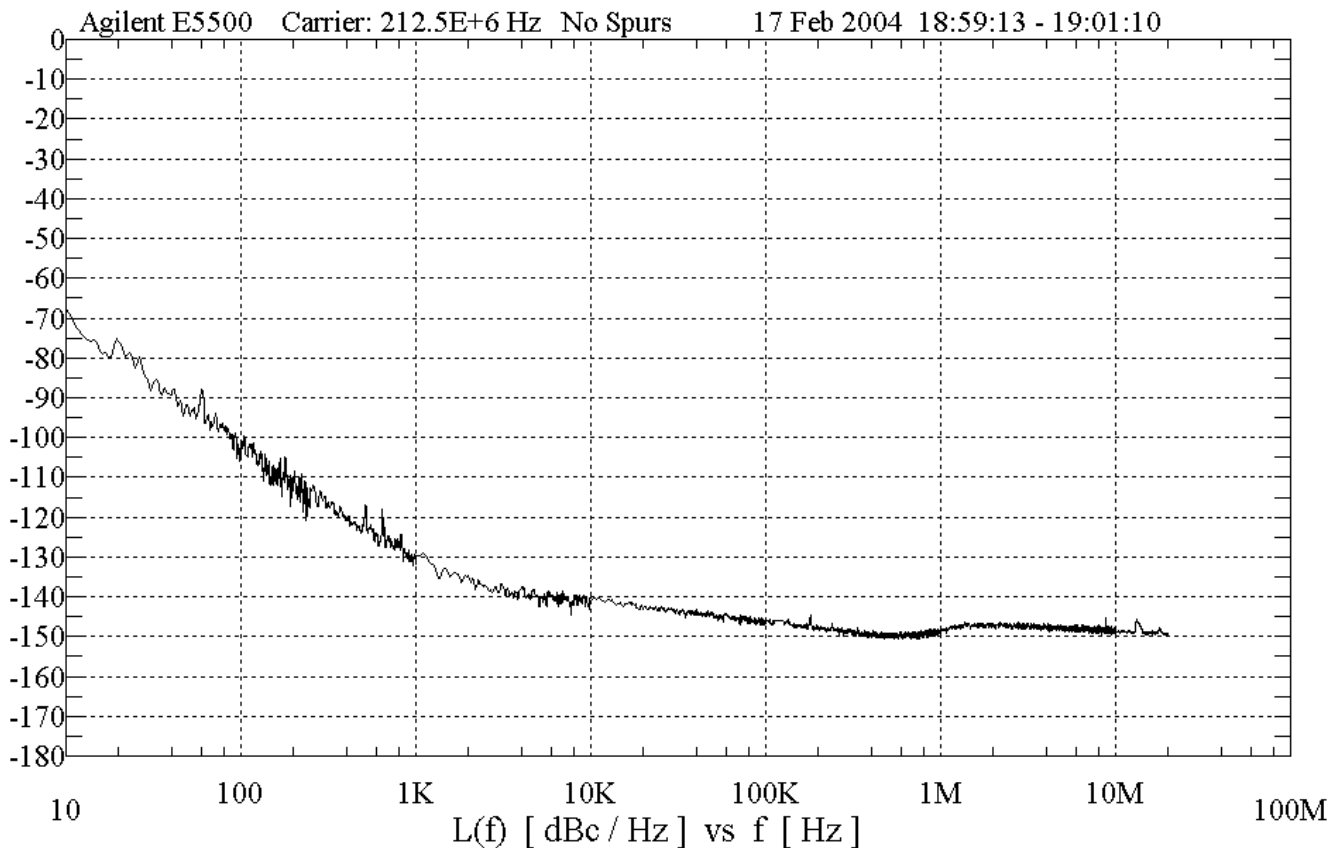


Figure 1: 2X AFM Phase Noise at 212.5 MHz (106.25 MHz 3rd overtone crystal)

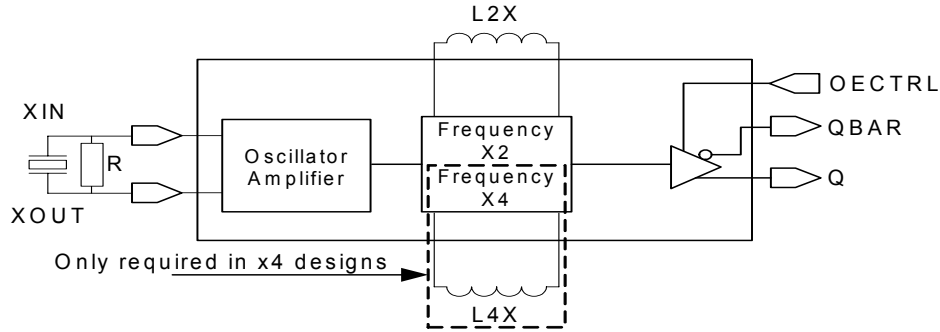


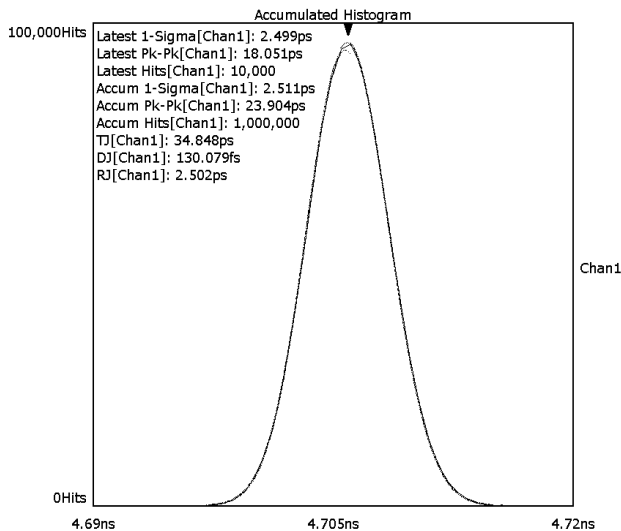
Figure 2: Overall XO AFM Block Diagram

FEATURES

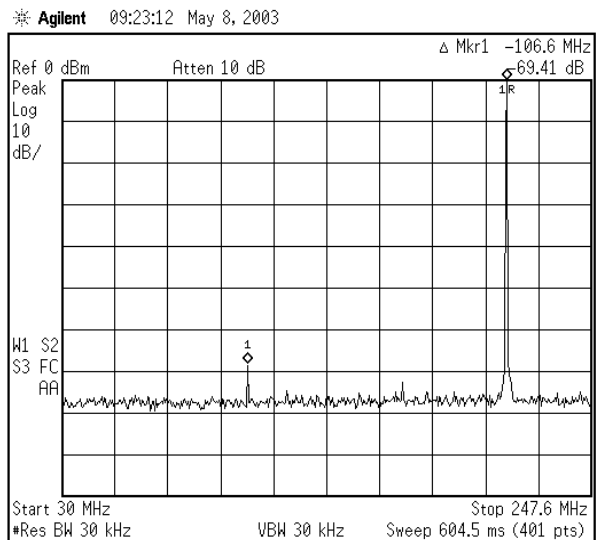
- Non Phase Locked Loop frequency multiplication
- Input frequency from 30-160 MHz
- Output frequency from 60-320-MHz
- Low Phase noise and jitter (equivalent to fundamental at the output frequency)
- Unbeatably low jitter
 - RMS phase jitter < 0.25ps (12kHz to 20MHz)
 - RMS period jitter < 2.5 ps Typ.
- Low Phase Noise
 - -145 dBc/Hz @ 100kHz Offset from 155.52MHz
 - -150 dBc/Hz @ 10MHz Offset from 155.52MHz
- Low input frequency eliminates the need for expensive crystals
- Differential output levels (PECL, LVDS), or single-ended CMOS
- Single 2.5V or 3.3V +/- 10% power supply
- Optional Industrial temperature range (-40°C to +85°C)
- Available in 16-pin SSOP, and 16-pin 3x3 QFN

Figure 3 shows the jitter histogram of the 2x Analog Frequency Multiplier at 212.50MHz, while figure 4 shows the very low levels of sub-harmonics that correspond to the exceptional performance (i.e. low jitter).

**Figure 3: Jitter Histogram at 212.5MHz
Analog Frequency Multiplier (2x)
with 106.25MHz crystal**



**Figure 4: Spectrum Analysis at 212.5MHz
Analog Frequency Multiplier (2x)
with sub-harmonic below -69 dBc**



PRODUCT SELECTOR GUIDE

FREQUENCY VERSUS PHASE NOISE PERFORMANCE

Part Number	Input Frequency Range (MHz)	Analog Frequency Multiplication Factor	Output Frequency Range (MHz)	Output Type	Phase Noise AT Frequency Offset From Carrier (dBc/Hz)							
					Carrier Freq. (MHz)	10 Hz	100 Hz	1 KHz	10 KHz	100 KHz	1 MHz	10 MHz
PL660-08	30 - 80	4	100 - 300	PECL	155.52	-72	-100	-125	-132	-142	-147	-149
PL660-09	30 - 80	4	100 - 300	LVDS	155.52	-72	-100	-125	-132	-142	-147	-149
PL663-07	30 - 80	2	60 - 160	PECL	156.25	-75	-105	-130	-140	-145	-150	-150
PL663-08	30 - 80	2	60 - 160	PECL	156.25	-75	-105	-130	-140	-145	-150	-150
PL663-09	30 - 80	2	60 - 160	LVDS	156.25	-75	-105	-130	-140	-145	-150	-150
PL663-17	75 - 140	2	150 - 280	CMOS	212.5	-70	-100	-130	-140	-145	-148	-148
PL663-18	75 - 140	2	150 - 280	PECL	212.5	-70	-100	-130	-140	-145	-148	-148
PL663-19	75 - 140	2	150 - 280	LVDS	212.5	-70	-100	-130	-140	-145	-148	-148
PL663-28	140 - 160	2	280 - 320	PECL	311.04	-60	-92	-122	-140	-142	-146	-146
PL663-29	140 - 160	2	280 - 320	LVDS	311.04	-60	-92	-122	-140	-142	-146	-148

Phase Noise numbers were obtained using Agilent 5500.

FREQUENCY VERSUS JITTER, AND SUB-HARMONIC PERFORMANCE

Part Number	Jitter Calc. Freq. (MHz)	RMS Period Jitter (ps)			Peak to Peak Period Jitter (ps)			RMS Accumulated (L.T.) Jitter (ps)			Phase Jitter (12 KHz-20MHz) (ps)			Spectral Specifications / Sub-harmonic Content (dBc)							
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Carrier Freq. MHz	Frequency (MHz)						
															@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)	
PL660-08	155.52		3	5		21	30			5		0.25		155.52	-66	-61				-67	-70
PL660-09	155.52		3	5		21	30			5		0.25		155.52	-66	-61				-67	-70
PL663-07	156.25		2	3		16	20			3		0.24		156.25		-70				-75	
PL663-08	156.25		2	3		16	20			3		0.24		156.25		-70				-75	
PL663-09	156.25		2	3		16	20			3		0.24		156.25		-70				-75	
PL663-17	212.50		2.5	4		18	20			4		0.19		212.50		-70				-75	
PL663-18	212.50		2.5	4		18	20			4		0.19		212.50		-70				-75	
PL663-19	212.50		2.5	4		18	20			4		0.19		212.50		-70				-75	
PL663-28	311.04		2.5	4		18	20			4		0.16		311.04		-65				-70	
PL663-29	311.04		2.5	4		18	20			4		0.16		311.04		-65				-70	

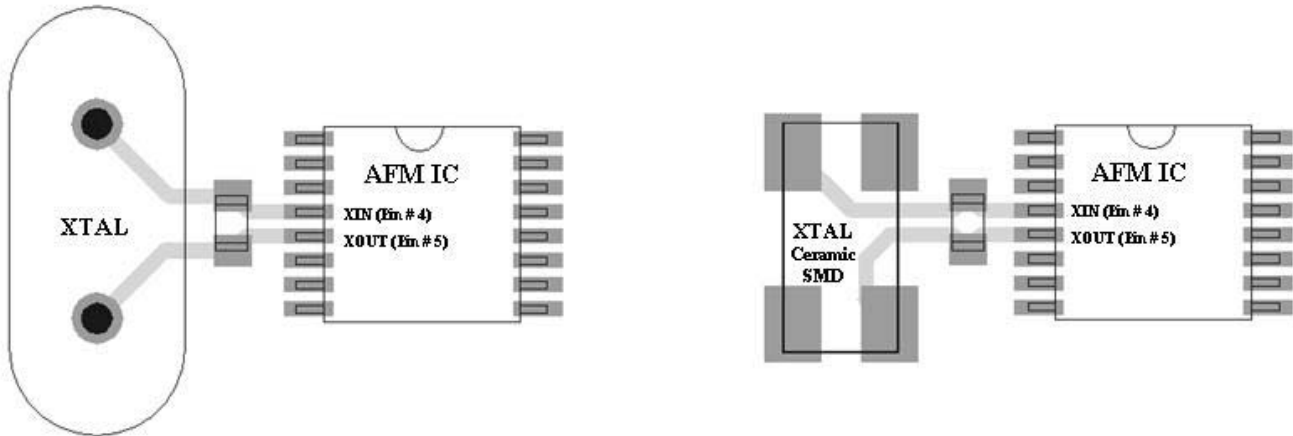
Note: Wavecrest Data 10,000 hits. No Filtering was used in Jitter Calculations.

Agilent 5500 was used for Phase Jitter Calculations.

Spectral Specifications were obtained using Agilent E7401A.

BOARD LAYOUT CONSIDERATIONS AND CRYSTAL SPECIFICATIONS

BOARD LAYOUT CONSIDERATIONS



To minimize parasitic effects, and improve performance:

- Place the crystal as close as possible to the IC.
- Make the board traces that are connected to the crystal pins symmetrical. The board trace symmetry is important, as it reduces the negative parasitic effects, for a clean frequency multiplication with low jitter.

CRYSTAL SPECIFICATIONS

Part Number	Crystal Resonator Frequency (F_{XIN})	Mode	CL (xtal)	ESR(R_E)	C_0	C_0/C_1
			Typical	Max.	Max.	Max.
PL660-08 PL660-09	25~75MHz	Fundamental or 3rd overtone	5pF	30 Ω	4.5pF	N.A.
PL663-07 PL663-08 PL663-09	30~80MHz	Fundamental or 3rd overtone	5pF	30 Ω	4.5pF	N.A.
PL663-17 PL663-18 PL663-19	75~140MHz	Fundamental or 3rd overtone	5pF	60 Ω	4.0pF	N.A.
PL663-28 PL663-29	140~160MHz	Fundamental or 3rd overtone	5pF	60 Ω	4.0pF	N.A.

Note: Non specified parameters can be chosen as standard values from crystal suppliers.
CL ratings larger than 5pF require a crystal frequency adjustment.
Request detailed crystal specifications from PhaseLink.

EXTERNAL COMPONENT VALUES - INDUCTOR SELECTION

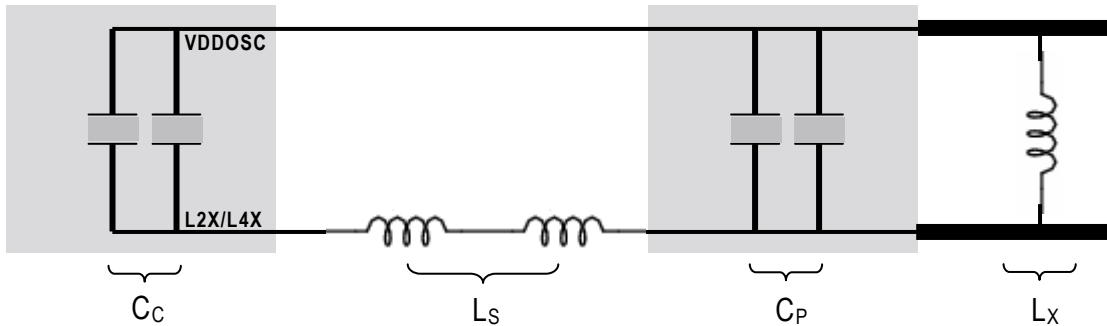


Figure 5: Diagram Representation Of The Related System Inductance And Capacitance

- C_C is the effective capacitance of the bond pad and the capacitor inside the IC.
- L_S is the effective parasitic inductance of the bond wire and the package lead frame/pins.
- C_P is the effective parasitic capacitance of the lead frame, and the board traces.
- L_X is the inductor value that needs to be determined for optimum performance.

INDUCTOR VALUE OPTIMIZATION

The required inductor value(s) for the best performance depends on the operating frequency, and the board layout specifications. The listed values in this datasheet are based on the calculated parasitic values from PhaseLink's evaluation board design (Gerber file available upon request). These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution. A method of determining the optimum inductor value(s) required in the system is described below to assist you in fine-tuning your system performance.

DETERMINING THE OPTIMUM INDUCTOR VALUE(S)

STEP 1

Refer to the 'Inductor Value vs. Output Frequency' table (below) to choose a starting value for the L2X inductor. Measure the signal's AC voltage swing on the L2X inductor. This can be accomplished by utilizing an oscilloscope, and a FET probe with <math><0.5\text{pF}</math> capacitance. The voltage swing can be as high as 3.5Vpp. You can achieve good performance at signal levels above 2.0Vpp, however best performance is achieved with signal levels approaching 3.0Vpp or higher. 1.5Vpp is required to observe an output signal. For the L4X inductor the signal levels should be at least 50% of the L2X signal levels mentioned above.

If at first you do not achieve the required voltage swing, try changing the inductor value to the next closest value and observe for performance improvement. A larger signal swing on the inductor indicates performance improvement, while smaller signal swing on the inductor indicates performance degradation. Try to find the inductor value where the signal levels are the largest.

Important Note: The signal level on L4X depends on the value of L2X inductor. You must set the L2X value first.

STEP 2

To fine-tune the inductor value(s) for the optimum performance, use a spectrum analyzer to observe the sub-harmonics. Measure the strength of all the sub-harmonics. Try changing the inductor value(s) to the next closest value and observe for performance improvement. You want to find the inductor value(s) where the harmonics are the lowest. Highest priorities are the $0.5 \times F_c$ and $1.5 \times F_c$ harmonics, since the jitter is most sensitive at these values.

Important Note: If your board design is significantly different than PhaseLink's evaluation board design, new parasitic values must be used to calculate the correct inductor value(s) that result in optimum performance. For additional information about determining the parasitic and optimum inductor value(s), please contact PhaseLink or visit us at [www.phaselink.com].

INDUCTOR VALUE VERSUS OUTPUT FREQUENCY (T)SSOP PACKAGE, BASED ON PHASELINK'S EVALUATION PCB

PL660-08/09				PL663-07/08/09		PL663-17/18/19		PL663-28/29	
L2X		L4X		L2X		L2X		L2X	
MHz	nH	MHz	nH	MHz	nH	MHz	nH	MHz	nH
60	159.15	120	64.73	60	134.55	150	54.49	150	54.49
62	148.63	124	60.32	62	125.59	155	50.62	155	50.62
64	139.09	128	56.32	64	117.46	160	47.10	160	47.10
66	130.39	132	52.67	66	110.05	165	43.90	165	43.90
68	122.45	136	49.34	68	103.29	170	40.97	170	40.97
70	115.19	140	46.29	70	97.10	175	38.30	175	38.30
72	108.52	144	43.49	72	91.42	180	35.84	180	35.84
74	102.38	148	40.92	74	86.19	185	33.57	185	33.57
76	96.72	152	38.54	76	81.37	190	31.49	190	31.49
78	91.49	156	36.34	78	76.92	195	29.56	195	29.56
80	86.64	160	34.30	80	72.79	200	27.77	200	27.77
82	82.15	164	32.41	82	68.97	205	26.11	205	26.11
84	77.97	168	30.65	84	65.41	210	24.57	210	24.57
86	74.08	172	29.01	86	62.10	215	23.13	215	23.13
88	70.45	176	27.48	88	59.01	220	21.79	220	21.79
90	67.06	180	26.05	90	56.13	225	20.53	225	20.53
92	63.89	184	24.72	92	53.43	230	19.36	230	19.36
94	60.92	188	23.46	94	50.90	235	18.26	235	18.26
96	58.13	192	22.28	96	48.53	240	17.23	240	17.23
98	55.51	196	21.17	98	46.30	245	16.26	245	16.26
100	53.05	200	20.13	100	44.20	250	15.34	250	15.34
102	50.73	204	19.14	102	42.23	255	14.48	255	14.48
104	48.54	208	18.21	104	40.37	260	13.67	260	13.67
106	46.47	212	17.33	106	38.61	265	12.90	265	12.90
108	44.52	216	16.50	108	36.95	270	12.17	270	12.17
110	42.67	220	15.71	110	35.38	275	11.48	275	11.48
112	40.92	224	14.96	112	33.89	280	10.83	280	10.83
114	39.26	228	14.25	114	32.48	285	10.21	285	10.21
116	37.69	232	13.58	116	31.14	290	9.62	290	9.62
118	36.19	236	12.94	118	29.87	295	9.07	295	9.07
120	34.77	240	12.32	120	28.66	300	8.53	300	8.53
122	33.42	244	11.74	122	27.51	305	8.03	305	8.03
124	32.13	248	11.18	124	26.42	310	7.54	310	7.54
126	30.90	252	10.65	126	25.38	315	7.08	315	7.08
128	29.73	256	10.14	128	24.39	320	6.64	320	6.64
130	28.61	260	9.65	130	23.44	325	6.22	325	6.22
132	27.54	264	9.18	132	22.53	330	5.81	330	5.81
134	26.52	268	8.74	134	21.67	335	5.43	335	5.43
136	25.54	272	8.31	136	20.84	340	5.06	340	5.06
138	24.61	276	7.89	138	20.05	345	4.70	345	4.70
140	23.71	280	7.50	140	19.29	350	4.36	350	4.36
142	22.85	284	7.11	142	18.56	355	4.03	355	4.03
144	22.03	288	6.75	144	17.86	360	3.72	360	3.72
146	21.24	292	6.39	146	17.20	365	3.41	365	3.41
148	20.48	296	6.05	148	16.55	370	3.12	370	3.12
150	19.75	300	5.72	150	15.94	375	2.84	375	2.84
152	19.05	304	5.40	152	15.35	380	2.57	380	2.57
154	18.38	308	5.09	154	14.78	385	2.31	385	2.31
156	17.73	312	4.79	156	14.23	390	2.06	390	2.06
158	17.10	316	4.50	158	13.70	395	1.81	395	1.81
160	16.50	320	4.22	160	13.20	400	1.58	400	1.58

Note: The industry standard inductor values may be different than the stated inductor values in the above table. Please select the closest industry standard inductor value and 'fine-tune' the system performance, as stated earlier. The listed inductor values, in the above table, are based on the calculated parasitic values from PhaseLink's evaluation board design. We recommend using high Q, small size 0402 or 0603 SMD inductors. Place the L2X inductor between pin L2X and the adjacent VDD pin and the L4X inductor between pins L4X and the adjacent VDD pin. For additional information about determining the parasitic and optimum inductor values, please contact PhaseLink or visit us at [www.phaselink.com].

EXTERNAL COMPONENT VALUES – 3RD OVERTONE RESISTOR SELECTIONS

This resistor is only required when a third overtone crystal is used. The chart below indicates the calculated and the nearest “E12” resistor values versus frequency.

PL660-08/09			PL663-07/08/09			PL663-017/18/19			PL663-28/29		
Freq. (MHz)	R3OT (Ω)	E12 Pick KΩ	Freq. (MHz)	R3OT (Ω)	E12 Pick KΩ	Freq. (MHz)	R3OT (Ω)	E12 Pick KΩ	Freq. (MHz)	R3OT (Ω)	E12 Pick KΩ
24	12,396	12	30	9,917	10	75	2,125	2.2	140.0	915	1.0
26	11,442	12	32	9,297	10	77.5	2,056	2.2	142.0	902	0.82
28	10,625	10	34	8,750	8.2	80	1,992	2.2	144.0	890	0.82
30	9,917	10	36	8,264	8.2	82.5	1,932	1.8	146.0	878	0.82
32	9,297	10	38	7,829	8.2	85	1,875	1.8	148.0	866	0.82
34	8,750	8.2	40	7,438	6.8	87.5	1,821	1.8	150.0	854	0.82
36	8,264	8.2	42	7,083	6.8	90	1,771	1.8	152.0	843	0.82
38	7,829	8.2	44	6,761	6.8	92.5	1,723	1.8	154.0	832	0.82
40	7,438	6.8	46	6,467	6.8	95	1,678	1.8	156.0	821	0.82
42	7,083	6.8	48	6,198	6.8	97.5	1,635	1.5	158.0	811	0.82
44	6,761	6.8	50	5,950	5.6	100	1,594	1.5	160.0	801	0.82
46	6,467	6.8	52	5,721	5.6	102.5	1,555	1.5			
48	6,198	6.8	54	5,509	5.6	105	1,518	1.5			
50	5,950	5.6	56	5,313	5.6	107.5	1,483	1.5			
52	5,721	5.6	58	5,129	4.7	110	1,449	1.5			
54	5,509	5.6	60	4,958	4.7	112.5	1,417	1.5			
56	5,313	5.6	62	4,798	4.7	115	1,386	1.5			
58	5,129	4.7	64	4,648	4.7	117.5	1,356	1.5			
60	4,958	4.7	66	4,508	4.7	120	1,328	1.2			
62	4,798	4.7	68	4,375	4.7	122.5	1,301	1.2			
64	4,648	4.7	70	4,250	3.9	125	1,275	1.2			
66	4,508	4.7	72	4,132	3.9	127.5	1,250	1.2			
68	4,375	4.7	74	4,020	3.9	130	1,226	1.2			
70	4,250	3.9	76	3,914	3.9	132.5	1,203	1.2			
72	4,132	3.9	78	3,814	3.9	135	1,181	1.2			
74	4,020	3.9	80	3,719	3.9	137.5	1,159	1.2			
76	3,914	3.9				140	1,138	1.2			

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

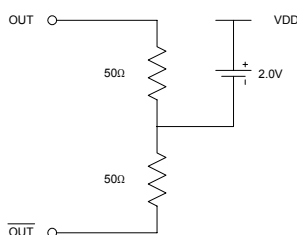
PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	T_S	-55	+150	°C
Ambient Operating Temperature	T_A	-40	+85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

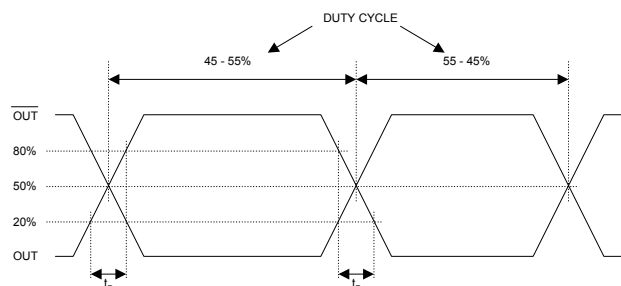
PECL ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (with loaded outputs)	I_{DD}	$F_{out} = 212.50\text{MHz}$	58	65	75	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Clock Duty Cycle		@ $V_{DD} - 1.3\text{V}$	45	50	55	%
Short Circuit Current				± 50		mA
Output High Voltage	V_{OH}	$R_L = 50\ \Omega$ to $V_{DD} - 2\text{V}$	$V_{DD} - 1.025$			V
Output Low Voltage	V_{OL}	$R_L = 50\ \Omega$ to $V_{DD} - 2\text{V}$			$V_{DD} - 1.620$	V
Clock Rise Time	t_r	@20/80%		0.4	0.7	ns
Clock Fall Time	t_f	@80/20%		0.4	0.7	ns

PECL Levels Test Circuit



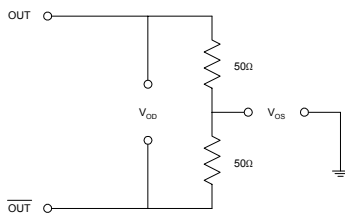
PECL Transition Time Waveform



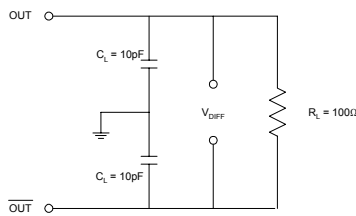
LVDS ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Current (with loaded outputs)	I_{DD}	$F_{out} = 212.50\text{MHz}$		55	60	mA	
Operating Voltage	V_{DD}		2.25		3.63	V	
Output Clock Duty Cycle		@ 1.25V	45	50	55	%	
Output Differential Voltage	V_{OD}	$R_L = 100\ \Omega$ (see figure)	247	355	454	mV	
VDD Magnitude Change	ΔV_{OD}		-50		50	mV	
Output High Voltage	V_{OH}			1.4	1.6	V	
Output Low Voltage	V_{OL}		0.9	1.1		V	
Offset Voltage	V_{OS}		1.125	1.2	1.375	V	
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV	
Power-off Leakage	I_{OXD}		$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}				-5.7	-8	mA
Differential Clock Rise Time	t_r	$R_L = 100\ \Omega$ $CL = 10\ \text{pF}$ (see figure)	0.2	0.5	0.7	ns	
Differential Clock Fall Time	t_f		0.2	0.5	0.7	ns	

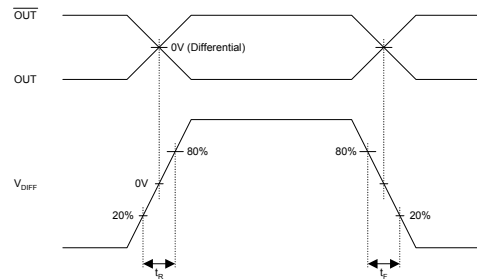
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform

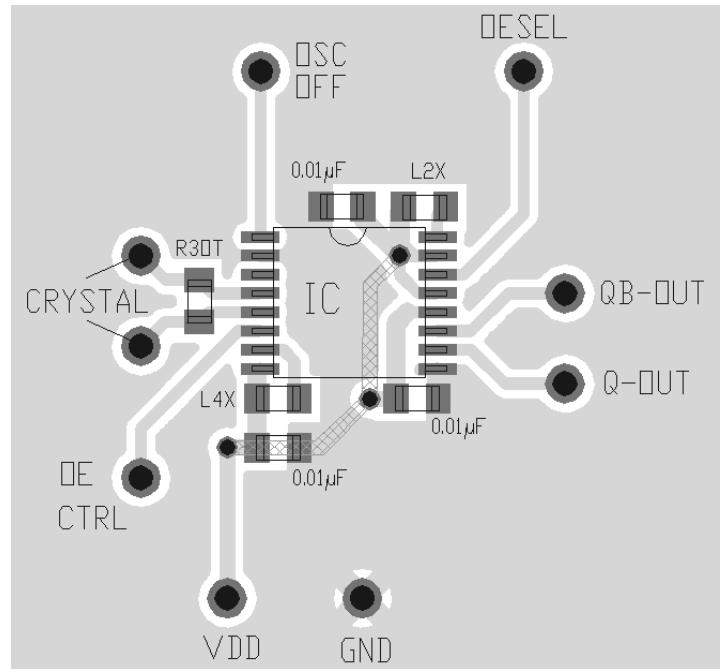


CMOS ELECTRICAL CHARACTERISTICS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise/Fall Time	10% ~ 90% VDD with 10 pF load		1.2	1.6	ns
Output Clock Duty Cycle	Measured @ 50% VDD	45	50	55	%
Short Circuit Current			± 50		mA

**BOARD LAYOUT DESIGN CONSIDERATIONS
FOR 4X AFMs**

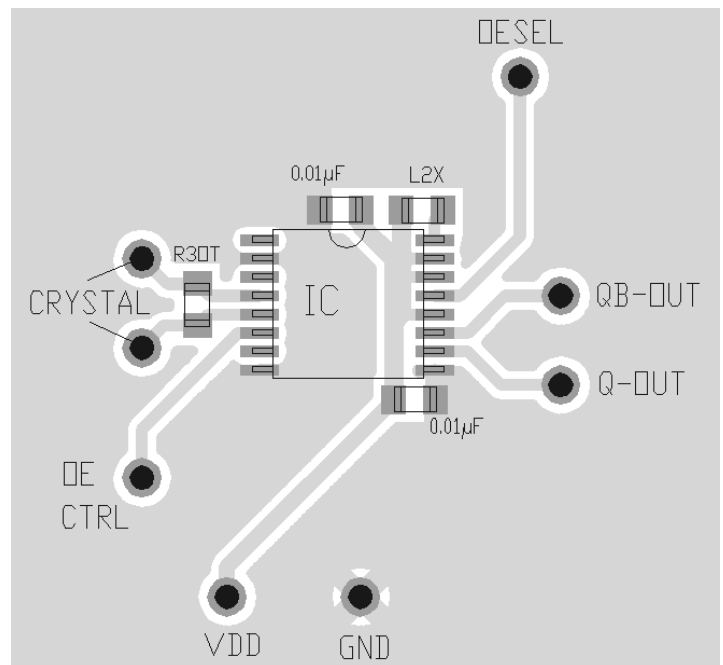
- Place L2X inductor as close as possible to the L2X [pin # 16], and the adjacent VDD [pin # 15].
- Place L4X inductor as close as possible to the L4X [pin # 7], and adjacent to VDD [pin # 8].
- Place a 0.01µF~0.1µF capacitor as close as possible to the VDDBUF [pin # 12] and GNDBUF [pin # 9].
- Place a 0.01µF~0.1µF capacitor as close as possible to the VDDOSC [pin # 15] and GNDOSC [pin # 2].
- Place a 0.01µF~0.1µF capacitor as close as possible to VDD [pin # 8] and GNDBUF [pin # 9].
- Place the crystal as close as possible to both crystal pins for the least cross-talk of the crystal signal to the output. **Important:** Crystal traces must be symmetrical.
- Try to avoid a direct connection between VDDBUF [pin # 12) and adjacent VDDANA [pin # 13], to prevent cross-talk from 0.5xFc into the output buffer.



Note: The R30T is only required when a third overtone crystal is used.

**BOARD LAYOUT DESIGN
CONSIDERATIONS FOR 2X AFMs**

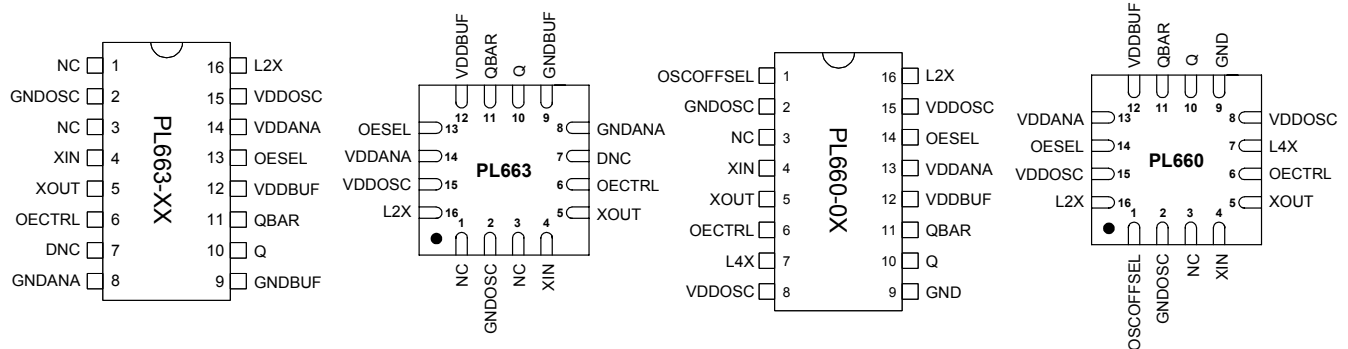
- Place L2X inductor as close as possible to the L2X [pin # 16], and the adjacent VDDOSC [pin # 15].
- Place a 0.01µF~0.1µF capacitor as close as possible to the VDDBUF [pin # 12] and GNDBUF [pin # 9].
- Place a 0.01µF~0.1µF capacitor as close as possible to the VDDOSC (Pin # 15) and GNDOSC (Pin # 2).
- Place the crystal as close as possible to both crystal pins for the least cross-talk of the crystal signal to the output. **Important:** Crystal traces must be symmetrical.



Note: The R30T is only required when a third overtone crystal is used.

Note: Please contact PhaseLink for the Gerber files of the above board layouts.

PACKAGE PIN DESCRIPTION AND ASSIGNMENT



PIN ASSIGNMENTS

Name	Pin #	Type	Product	Description
OSCOFFSEL	1	I	2X	No connection.
			4X	Set to "0" (GND) to turn off the oscillator when outputs are disabled (OE). Default (no connect) is OSC always on.
GNDOSC	2	P	2X & 4X	GND connection for oscillator.
VCON	3	I	2X	No connection.
			4X	Control Voltage input. Use this pin to change the output frequency by varying the applied Control Voltage.
XIN	4	I	2X & 4X	Input from crystal oscillator circuitry.
XOUT	5	O	2X & 4X	Output from crystal oscillator circuitry.
OECTRL	6	I	2X & 4X	Output Enable input. See "OE LOGIC SELECTION TABLE".
L4X	7	I	2X	DNC (Do Not Connect).
			4X	External inductor connection. The inductor is recommended to have a high Q value and must be placed between L2X and VDD.
VDDOSC	8	P	2X	VDD connection for oscillator circuitry. VDDOSC should be separately decoupled from other VDDs whenever possible.
GNDANA			4X	GND connection.
GNDBUF	9	P	2X & 4X	GND connection.
Q	10	O	2X & 4X	PECL/LVDS/CMOS output.
QBAR	11	O	2X & 4X	Complementary PECL/LVDS output or in phase CMOS.
VDDBUF	12	P	2X & 4X	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
OESEL	13	I	2X	Selector input to choose the OE control logic (see "OE SELECTION TABLE").
	14		4X	
VDDANA	14	P	2X	VDD connection for analog circuitry. VDDANA should be separately decoupled from other VDDs whenever possible.
	13		4X	
VDDOSC	15	P	2X & 4X	VDD connection for oscillator. VDD should be separately decoupled from other VDDs whenever possible.
L2X	16	I	2X & 4X	External inductor connection. The inductor is recommended to have a high Q value and must be placed between L2X and VDD.

Note: 663-xx devices are 2x multipliers, and 660-xx devices are 4x multipliers.

OE LOGIC SELECTION

OUTPUT	OESL	OE	Output State
PECL	0 (Default)	0 (Default)	Enabled
		1	Tri-state
	1	0	Tri-state
		1 (Default)	Enabled
LVDS or CMOS	0 (Default)	0	Tri-state
		1 (Default)	Enabled
	1	0 (Default)	Enabled
		1	Tri-state

OESL and OE: Connect to VDD to set to "1", connect to GND to set to "0". [The 'Default' state is set by internal pull up/down resistor.]

PACKAGE INFORMATION

16 PIN SSOP

16 PIN SSOP (inch)

Symbol	SSOP		
	Min.	Nom.	Max.
A	.053	.064	.069
A1	.004	.006	.010
B	.008	-	.012
C	.007	-	.010
D	.189	.193	.197
E	.150	.154	.157
H	.228	.236	.244
L	.016	.025	.050
e	.025 BASIC		

16 PIN 3x3 QFN

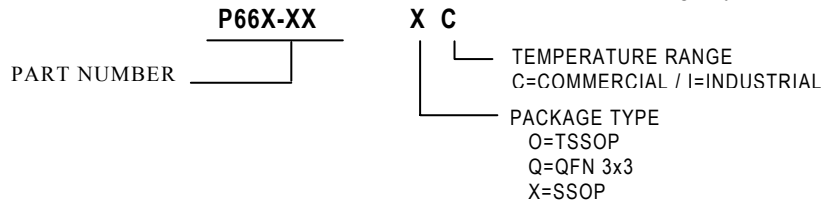
VARIATIONS:

SYMBOL	16 LD		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		

Important note: QFN package pin 1 indicator is metallized and connected to GND through the leadframe.

ORDERING INFORMATION

Note: The order number for this device is a combination of Device number, Package type and Operating temperature range.



Order Number	Marking	Package Option
PL66X-XXOC-R	P66X-XX OC	TSSOP – Tape and Reel
PL66X-XXQC-R	P66X-XX	QFN – Tape and Reel
PL66X-XXXC-R	P66X-XX XC	SSOP – Tape and Reel
PL66X-XXOC	P66X-XX OC	TSSOP – Tube
PL66X-XXQC	P66X-XX	QFN – Tube
PL66X-XXXC	P66X-XX XC	SSOP – Tube

ORDERING INFORMATION

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by PhaseLink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY

PhaseLink’s products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.

PhaseLink Offices

PhaseLink Corporation, USA

47745 Fremont Boulevard
Fremont, CA 94538
+ 1.510.492.0990 (phone)
+ 1.510.492.0991 (fax)
salesinfo@phaselink.com
<http://www.phaselink.com>

PhaseLink Company, Ltd., Taiwan

Asia Headquarters
5F-2, No. 94, Pao Chung Road.
Hsin Tien, Taipei, Taiwan, R.O.C.
+ 886.2.2910.0248 (phone)
+ 886.2.2910.0249 (fax)
salesinfo@phaselink.com
<http://www.phaselink.com>

PhaseLink Corporation, Japan

1-38-7-111 Matsubara Setagaya-ku
Tokyo 156-0043
+ 81-3-5355-0536 (phone)
+81-3-5355-0553 (fax)
salesinfo@phaselink.com
<http://www.phaselink.com>

PhaseLink Corporation, China

17F,Block 2,Conrad Garden,Caltian
Rd
Futian,ShenZhen , PRC 518033
+86-755-83020204 (phone)
+86-755-83020207 (fax)
salesinfo@phaselink.com
<http://www.phaselink.com>