PETERMANN TECHNIK
your clocking experts

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ULTRA-LOW POWER OSCILLATOR 1-26MHz

SERIES „ULPO“

FEATURES

+ Ultra Low Power High Precision Oscillator for Low Cost
+ Excellent long time reliability
+ Ultra-small 1.5 mm x 0.8 mm package
+ 1 to 26 MHz with 6 decimal places of accuracy
+ Ultra low power consumption of 50 µA at 2.048 MHz
+ Operating temperature from -40°C to 85°C (ask for –40/+105°C)
+ RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free / MSL1@260°

DESCRIPTION AND APPLICATIONS

The ULPO is the industry's smallest and the lowest power MHz oscillator. With it's ultra low power consumption, the ULPO enables longer battery life time for a wearable, IoT or mobile device compared to a quartz-based oscillator or resonator.
The combination of lowest power, smallest package and flexible output frequency makes it ideal for power sensitive and space constrained applications including:

+ Smart Phones
+ Tablets
+ Ultra-Small Notebook PC
+ Battery powered devices
+ Wearables
+ IoT devices
+ GPS
+ Smart Metering
+ Sport video cams
+ Home Automation
+ Health and Medical monitoring
+ Hearing aids

GENERAL DATA[1,2]

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
FREQUENCY RANGE						
Output Frequency Range	F	1	-	26	MHz	Standard frequencies (See Table 1.)
FREQUENCY STABILITY AND AGING						
Initial Tolerance	F_tol	-15	-	+15	PPM	Frequency offset at 25°C post reflow
Frequency Stability	F_stab	-100	-	+100	PPM	Inclusive of initial tolerance, and variations over operating temperature, rated power supply voltage and output load. Contact PETERMANN-TECHNIK for ±25 or ±50 ppm options.
First Year Aging	F_1 year	-3	-	+3	PPM	At 25°C
OPERATING TEMPERATURE RANGE						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial. Contact PETERMANN-TECHNIK for –40°C to 105°C option.
Storage Temperature Range	T_stor	-55	–	+125	°C	Storage
SUPPLY VOLTAGE AND CURRENT CONSUMPTION						
Supply Voltage	V_{DD}	1.62	1.8	1.98	V	
		2.25	–	3.63	V	Any voltage from 2.25 to 3.63V.
Current Consumption	I_{DD}	–	60	–	µA	f = 3.072 MHz, V_{DD} = 1.8V, no load
		–	110	130	µA	f = 6.144 MHz, V_{DD} = 1.8V, no load
		–	230	270	µA	f = 6.144 MHz, V_{DD} = 1.8V, 10 pF load
		–	–	160	µA	f = 6.144 MHz, V_{DD} = 2.25V to 3.63V, no load
		–	160	–	µA	f = 12 MHz, V_{DD} = 1.8V, no load
Standby Current	I_std	-	0.7	1.3	µA	V_{DD} = 1.8V, ST pin = HIGH, output is weakly pulled down
		–	–	1.5	µA	V_{DD} = 2.25V to 3.63V, ST pin = HIGH, output is weakly pulled down
LVCMOS OUTPUT CHARACTERISTICS						
Duty Cycle	DC	45	-	55	%	
Rise/ Fall Time	T_r, T_f	-	4	8	ns	V_{DD} = 1.8V, 20% - 80%. Contact PETERMANN-TECHNIK for other programmable rise/fall options
		-	-	8		V_{DD} = 2.25V to 3.63V, 20% - 80%. Contact PETERMANN-TECHNIK for other programmable rise/fall options
Output High Voltage	VOH	90%	-	-	V_{DD}	IOH = -0.5 mA (V_{DD} = 1.8V) IOH = -1.2 mA (V_{DD} = 2.25V to 3.63V)
Output Low Voltage	VOL	-	-	10%	V_{DD}	IOL = 0.5 mA (V_{DD} = 1.8V) IOH = 1.2 mA (V_{DD} = 2.25V to 3.63V)

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GENERAL DATA (continued)

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
INPUT CHARACTERISTICS						
Input High Voltage	VIH	80%	-		VDD	
Input Low Voltage	VIL	-	-	20%	VDD	
Input Slew Rate	In-slew	10	-	-	V/µs	
Input Pull-down Impedance	Z_in	300	-	-	kΩ	Active mode (ST pin = LOW), V_{DD} = 1.8V
		270	-	-	kΩ	Active mode (ST pin = LOW), V_{DD} = 2.25V to 3.63V
		2.5	-	-	MΩ	Standby mode (ST pin = HIGH), V_{DD} = 1.8V
		1.3	-	-	MΩ	Standby mode (ST pin = HIGH), V_{DD} = 2.25V to 3.63V
LVCMOS OUTPUT (STANDARD VERSION)						
Startup Time	T_start	-	75	150	ms	Measured from the time V_{DD} reaches 90% of its final value
Startup Time	T_stdby	-	-	20	µs	Measured from the time ST pin crosses 50% threshold
Resume Time	T_resume	-	2	3	ms	Measured from the time ST pin crosses 50% threshold
JITTER PERFORMANCE						
RMS Period Jitter	T_jitt	-	75	110	ps	f = 6.144 MHz, V_{DD} = 1.8V
		-	-	110	ps	f = 6.144 MHz, V_{DD} = 2.25V to 3.63V
RMS Phase Jitter	T_phj	-	0.8	2.5	ns	f = 6.144 MHz, V_{DD}= 1.8V, Integration bandwidth = 100 Hz to 40 kHz [2]
		-	-	2.5	ns	f = 6.144 MHz, V_{DD} = 2.25V to 3.63V, Integration bandwidth = 100 Hz to 40 kHz [2]

Notes:
1. Current consumption with load is a function of the output frequency and output load. For any given output frequency, the capacitive loading will increase current consumption equal to C_load*V_{DD}*f(MHz).
2. Max spec inclusive of 25 mV peak-to-peak sinusoidal noise on V_{DD}. Noise frequency 100 Hz to 20 MHz.
3. Do not use cleaning baths operating at ultrasonic frequencies.

TABLE 1. STANDARD FREQUENCES

STANDARD FREQUENCIES	
2.048 MHz	12.288 MHz
4 MHz	16 MHz
6.144 MHz	19.2 MHz
8 MHz	24 MHz
12 MHz	26 MHz

PIN DESCRIPTION

PIN	SYMBOL	I/O	FUNCTIONALITY
1	ST	Input	L: Specified frequency output H: Output is low (weak pull down). Device goes to the standby mode. Supply current reduces to I_std.
2	OUT	Output	LVCMOS clock output
3	V_{DD}	Power	Supply voltage. Bypass with a 0.01µF X7R capacitor.
4	GND	Power	Connect to ground

FIGURE 1. PIN ASSIGNMENTS (TOP VIEW)

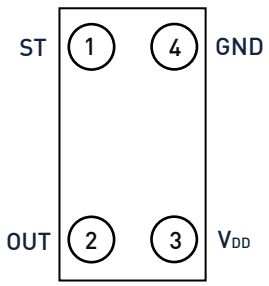

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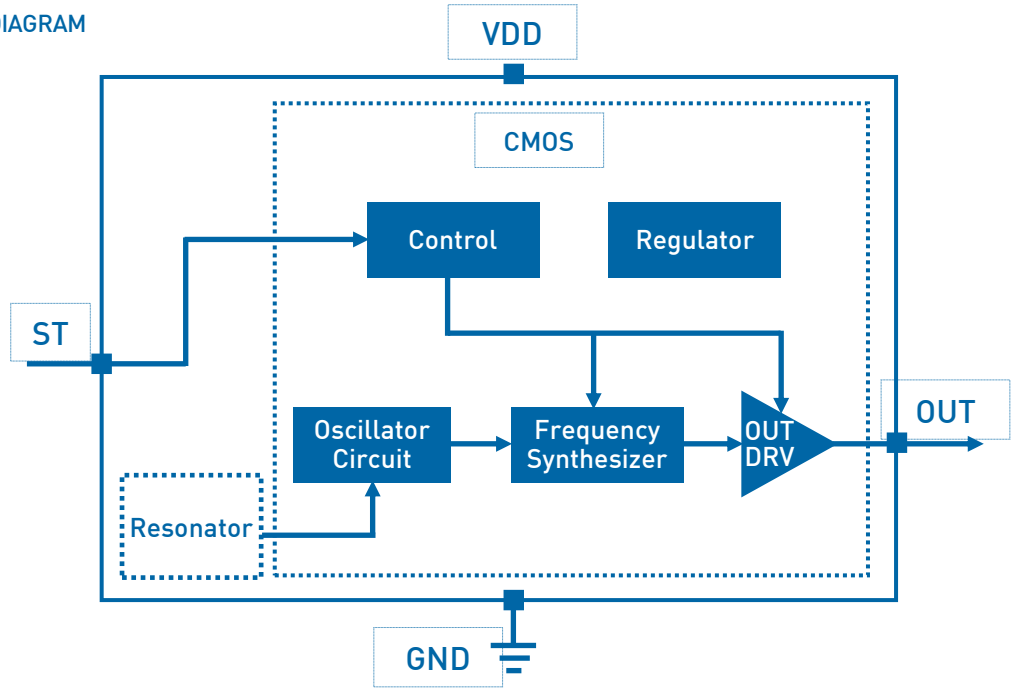
FIGURE 2. BLOCK DIAGRAM



DEVICE OPERATING MODES AND OUTPUTS

The ULPO supports ≤0.7 µA standby mode for battery-powered and other power sensitive applications. The switching between the active and standby modes is controlled by the logic level on the ST pin.

TABLE 2. OPERATING MODES AND OUTPUT STATES

ST Pin	Mode	OUTPUT	Max Current Consumption
LOW	Active	Specified frequency	60 µA @ 3.072 MHz
FLOAT	Active with 200 kΩ internal pull-down	Specified frequency	60 µA @ 3.072 MHz
HIGH	Standby	Hi-Z pulled-down with 1MΩ impedence	1.3 µA

ACTIVE MODE

The ULPO operates in the active mode when the ST pin is at logic LOW or FLOAT. In the active mode, the device uses the on-chip frequency synthesizer to generate an output from the internal resonator reference. The frequency of the output is factory programmed based on the device ordering code.

STANDBY MODE

The ULPO operates in the standby mode when the ST pin is at logic HIGH. In the standby mode, all internal circuits with the exception of the oscillator circuit and the ST pin detection logic are turned off to reduce power consumption. While in standby mode, the input impedance of the ST pin is increased to further reduce system level power consumption. The output driver of the device in the standby mode is weakly pulled-down with a 1 MΩ impedance.

OUTPUT DURING STARTUP AND RESUME

The ULPO starts up with the output disabled. The output is enabled once all internal circuit blocks are active, and logic LOW or FLOAT is detected on the ST pin.

As shown in Table 2, logic HIGH at ST pin forces the ULPO into "standby" state, causing the output to disable. Upon pulling ST pin LOW, the device enters "resume" state, keeping the output disabled. Once "resume" state ends, the device output enables. The first clock pulse after startup or resume is accurate to the rated stability.

LOW POWER DESIGN GUIDELINES

For high EM noise environments, we recommend the following design guidelines:

+ Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
+ Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the oscillator.
+ Place a solid GND plane underneath the oscillator to shield the oscillator from noisy traces on the other board layers.

MANUFACTURING GUIDELINES

+ No Ultrasonic or Megasonic Cleaning: Do not subject the ULPO to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
+ Applying board-level underfill (BLUF) to the device is acceptable, but will cause a slight shift of few PPM in the initial frequency tolerance. Tested with UF3810, UF3808, and FP4530 underfill.
+ Reflow profile, per JESD22-A113D.

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TEST CIRCUIT AND WAVEFORM

FIGURE 3. TEST CIRCUIT

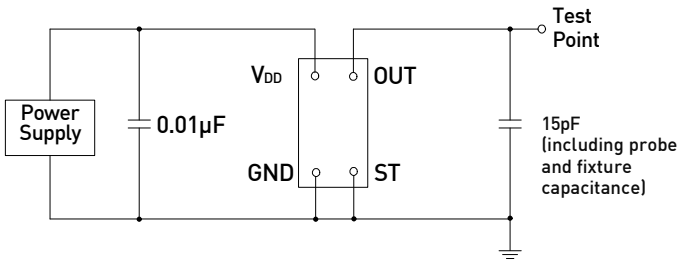
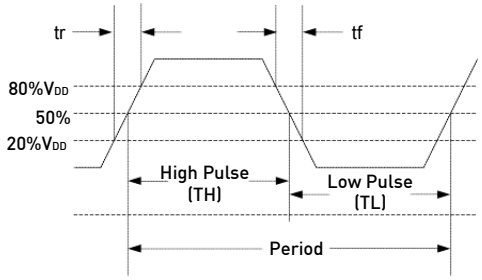


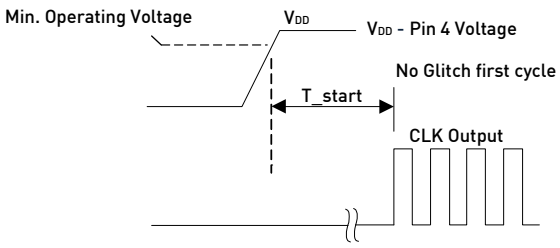
FIGURE 4. WAVEFORM[4]



Notes:
4. Duty Cycle is computed as Duty Cycle = TH/Period

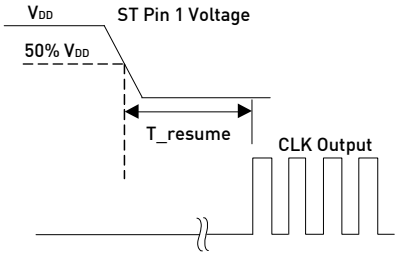
TIMING DIAGRAMS

FIGURE 5. STARTUP TIMING[5, 6]



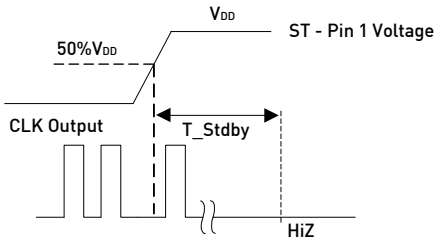
T_start: Time to valid clock output from power on

FIGURE 6. RESUME TIMING[6, 7]



T_resume: Time to valid clock output from the time ST pin crosses 50% threshold

FIGURE 7. STANDBY TIMING[6]



T_Stdby: Time for output to go high-Z from the time ST pin crosses 50% threshold

Note:
5. ULPO supports no runt pulses and no glitches during startup or resume.
6. Supports gated output which is accurate within rated frequency stability from the first cycle.

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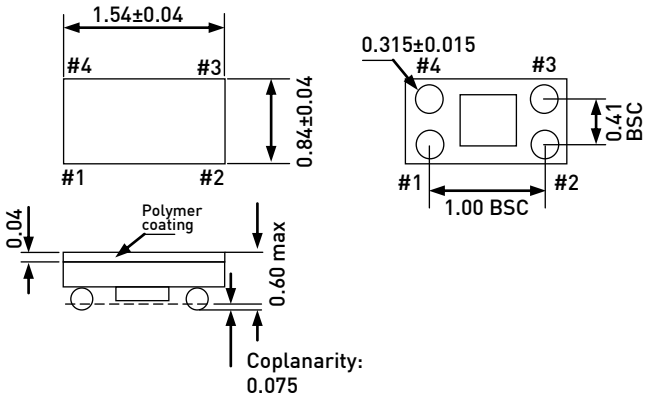
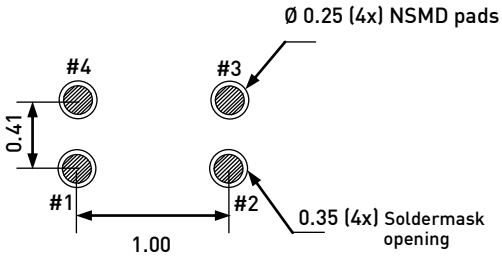
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

1.5 X 0.8 MM



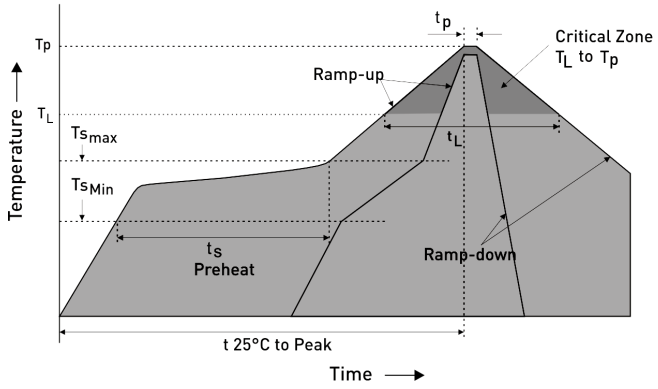
RECOMMENDED LAND PATTERN (UNIT:MM)



(soldermask openings shown with heavy dashed line)

Recommended 4-mil (0.1mm) stencil thickness

REFLOW SOLDER PROFILE



IPC/JEDEC Standard	IPC/JEDEC JESD22-A113D
Moisture Sensitivity Level	Level 1
TS MAX to TL (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (TS MIN)	150°C
- Temperature Typical (TS TYP)	175°C
- Temperature Maximum (TS MAX)	200°C
- Time (tS)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (TL)	60 - 150 Seconds
Peak Temperature (TP)	255°C Maximum
Target Peak Temperature (TP Target)	250°C
Time within 5°C of actual peak (tP)	20 - 40 seconds
Max. Number of Reflow Cycles	3
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum

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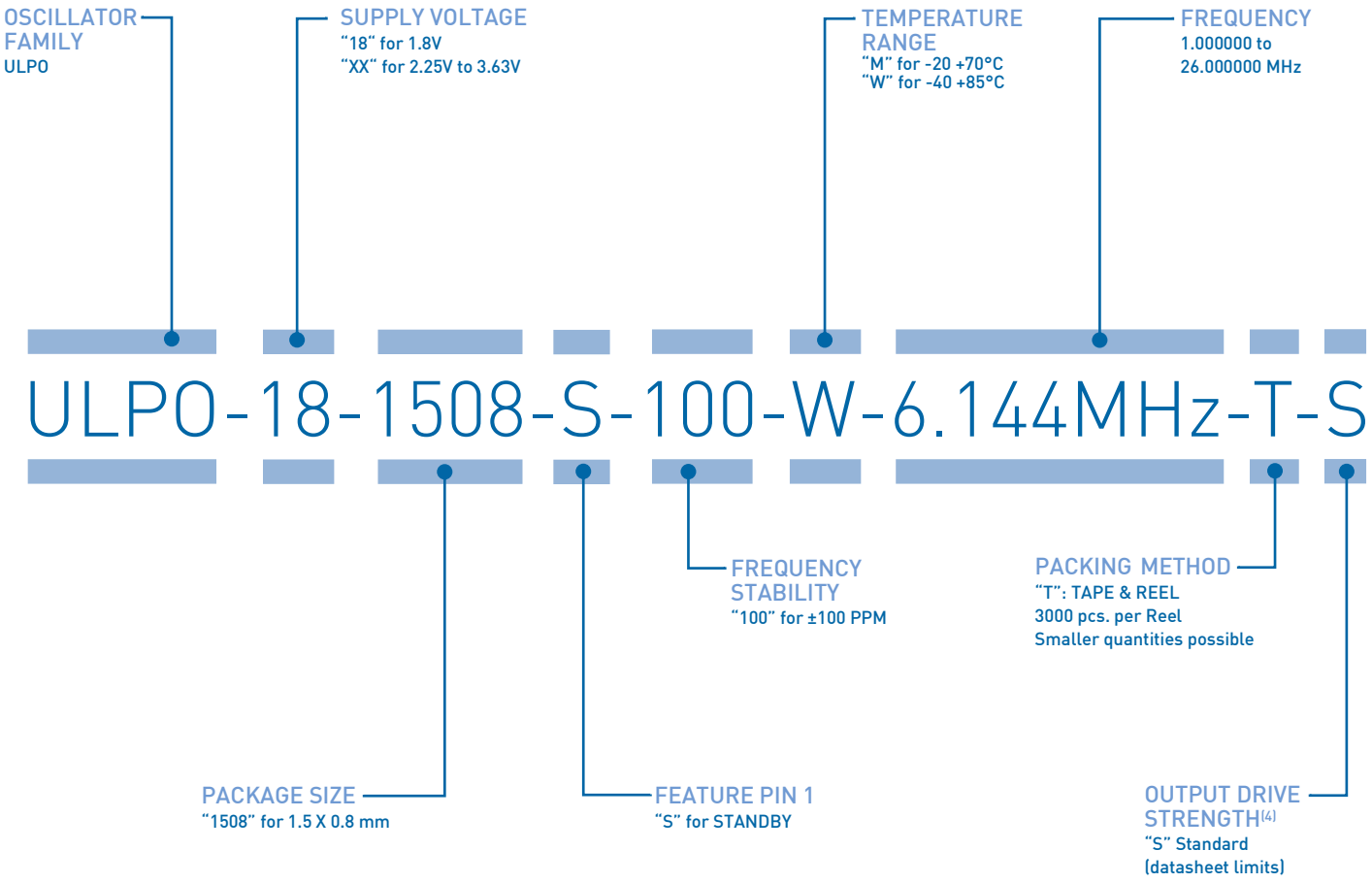
ORDERING INFORMATION



Notes:
Contact PETERMANN-TECHNIK for other drive strength options that result in different rise/fall time for any given output load.

EXAMPLE: ULPO-18-1508-S-100-W-6.144MHz-T-S

PLEASE CLICK HERE TO CREATE YOUR OWN ORDERING CODE

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REVISION HISTORY

REVISION	RELEASE DATE	AMENDMENTS SUMMARY
00	OKTOBER 2015	+ Initial Data Sheet (SPEC 01/REV.00)
01	MARCH 2016	+ Revised initial tolerance, current consumption, standby current, input high/low voltage for ST, input pull-down impedance, startup/resume time and RMS period/phase jitter in Table General Data. + Added standard additional operating temperature range (–40°C to 105°C) + Added typ. current consumption
02	JUNE 2018	+ Added 2.25V - 3.63 V option + Revised Current Consumption + Revised Dimensions and Patterns

PREMIUM QUALITY BY PETERMANN-TECHNIK

DMSZ certified according to ISO 9001 QM 00886

OUR COMPANY IS CERTIFIED ACCORDING TO ISO 9001:2015 IN OCTOBER 2016 BY THE DMSZ CERTIFIKATION GMBH AND CERTIFIED ACCORDING TO 14001:2015 IN MARCH 2018 BY SEQ-CERT.

THIS IS FOR YOU TO ENSURE THAT THE PRINCIPLES OF QUALITY MANAGEMENT ARE FULLY IMPLEMENTED IN OUR QUALITY MANAGEMENT SYSTEM AND QUALITY CONTROL METHODS ALSO DOMINATE OUR QUALITY STANDARDS.